REMARKS

In response to the Office action and the Advisory Action, applicant has amended the Specification. For example, in paragraph **[0017]**, it is now stated that "[t]he substrate 1 is a transparent substrate", and that "[t]he gate electrode 2 controls the TFT 200 to switch on or off, and the TFT 200 is applied to a single-gated transistor". Applicant submits that the altered descriptions merely state explicitly what was already implicit in the disclosure at the time of filing of the original Specification. That is, a person of ordinary skill in the art would have understood the content of the altered descriptions from a reading of the original specification. Therefore applicant submits that no new matter is entered. Further, in paragraph **[0020]**, certain advantages are now stated. Applicant submits that the stated advantages would be appreciated by a person of ordinary skill in the art from a reading of the disclosure regarding the thin film transistor of the present invention as contained in originally filed Specification. Therefore no new matter is entered.

Further, applicant has amended claims 1, 2, 7, 11 and 21, and has added new claims 22-27. Applicant submits that no new matter is entered.

Claim Rejections under 35 U.S.C. 103

Claims 1-2, 4-6, 8-10 and 21 are rejected under 35 U.S.C. 103(a) as being anticipated by Denton et al. ("Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI islands with an Isolated Buried Polysilicon Backgate", IEEE Electron Device Letters, Vol. 17, No. 11, November 1996, pgs. 509-511) in view of Hiramatsu et al. (U.S. Pat. 5,311,040).

Examiner states that "Denton (FIG. 1) discloses a thin film transistor, comprising: a substrate; [and] a gate electrode (polysilicon bottom gate) disposed in the substrate..." Examiner further states that "Hiramatsu (FIG. 1) discloses a gate electrode 2, which is made of Ta or MoTa (column 3, lines 25-26) in order to increase conductivity of the semiconductor gate electrode."

In response to the rejection, applicant has, inter alia, amended independent claims 1 and 21. Applicant asserts that the amended claims are now patentable, as follows:

Amended claim 1 recites in pertinent part "a thin film transistor used in a display device, comprising: a **transparent substrate; a gate electrode being made of metallic material, and the gate electrode disposed in the transparent substrate.**"

Firstly, the thin film transistor disclosed by Denton comprises a bottom gate disposed in a **silicon substrate** and made of polysilicon, whereas the thin film transistor of amended claim 1 comprises **a gate electrode made of metallic material, the gate electrode being disposed in the transparent substrate.** Secondly, the thin film transistor disclosed by Denton further comprises a top gate. That is, the thin film transistor disclosed by Denton is a dual-gated thin film transistor controlled by two gates, whereas the thin film transistor of amended claim 1 is a thin film transistor controlled by one gate electrode. These differences indicate that Denton does not teach a thin film transistor comprising all the limitations recited in amended claim 1.

Further, Hiramatsu does not disclose a thin film transistor including **a gate electrode disposed in a transparent substrate**.

Therefore, there is no motivation or suggestion in either Denton or Hiramatsu that the reference be combined with the other in such a way as to provide a thin film transistor comprising all the limitations recited in amended claim 1.

Moreover, the thin film transistor of amended claim 1 produces new and unexpected results. That is, **the gate electrode made of metallic material is deposited in the transparent substrate**, and thus the thickness of the gate electrode can be changed by changing the depth of the transparent substrate etched. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that the thin film transistor of amended claim 1 can efficiently reduce an RC (resistance-capacitance) delay of a scanning signal. Compare this with Denton, wherein the polysilicon backgate has applications as a bias to dynamically shift topgate threshold voltage for low power circuits.

Accordingly, amended claim 1 is submitted to be unobvious and patentable over Denton in view of Hiramatsu under 35 U.S.C. 103(a). Reconsideration and withdrawal of the rejection of amended claim 1 are respectfully requested.

Claims 2, 4-6 and 8-10 depend directly and indirectly from independent amended claim 1, and therefore should also be allowable.

For reasons similar to those asserted above in relation to amended claim 1, it is submitted that Denton combined with Hiramatsu does not

disclose, teach or suggest all the limitations of the thin film transistor of the display device recited in amended claim 21.

Accordingly, amended claim 21 is submitted to be unobvious and patentable over Denton in view of Hiramatsu under 35 U.S.C. 103(a). Reconsideration and withdrawal of the rejection and allowance of amended claim 21 are respectfully requested.

Claims 1-2, 4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (U.S. Pat. 6,423,578) in view of Hiramatsu et al. (U.S. Pat. 5,311,040).

Examiner states that "Maeda (FIG. 9) discloses a thin film transistor comprising: a substrate 50a, [and] a gate electrode 41 disposed in the substrate 50a..." Examiner further states that "Hiramatsu (FIG. 1) discloses a gate electrode 2, which is made of Ta or MoTa (column 3, lines 25-26) in order to increase conductivity of the semiconductor gate electrode."

Amended claim 1 recites in pertinent part a thin film transistor used in a display device, comprising: a **transparent substrate; a gate electrode made of metallic material, the gate electrode being disposed in the transparent substrate**; and a gate insulation layer disposed on the transparent substrate and the gate electrode.

Applicant asserts that the rejected claims are now patentable, as follows:

As regards claim 1, Maeda (FIG. 9) discloses that a double-gate field

effect transistor having four electrodes comprises a first support substrate 10, a lower gate 41 positioned on the side of the first support substrate 10, an insulator 50a, and an upper gate 81, wherein the lower gate electrode 41 is embedded in the insulator 50a (column 4, lines 18-23). That is, the double-gate field effect transistor disclosed by Maeda is controlled by an upper gate 81, and a lower gate 41 positioned on the side of the first support substrate 10. However, the thin film transistor of amended claim 1 comprises **a gate electrode made of metallic material disposed in the transparent substrate**. Thus, the thin film transistor of amended claim 1 is controlled by a single gate electrode. These differences indicate that Maeda does not teach a thin film transistor comprising all the limitations recited in amended claim 1.

Further, Hiramatsu does not disclose a thin film transistor including **a gate electrode disposed in a transparent substrate**.

Therefore, there is no motivation or suggestion in either Maeda or Hiramatsu that the reference be combined with the other in such a way as to provide a thin film transistor comprising all the limitations recited in amended claim 1. Moreover, the thin film transistor of amended claim 1 produces new and unexpected results. That is, **the gate electrode made of metallic material is deposited in the transparent substrate**, and thus the thickness of the gate electrode can be changed by changing the depth of the transparent substrate etched. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that the thin film transistor of amended claim 1 can efficiently reduce an RC (resistance-capacitance) delay of a scanning signal.

Accordingly, amended claim 1 is submitted to be unobvious and

patentable over Maeda in view of Hiramatsu under 35 U.S.C. 103(a). Reconsideration and withdrawal of the rejection and allowance of amended claim 1 are respectfully requested.

Claims 2, 4 and 6-7 depend directly from independent amended claim 1, and therefore should also be allowable.

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denton et al. in view of Hiramatsu (U.S. Pat. 5,311,040) and further in view of Honda (U.S. Pat. 6,639,246).

Examiner states that "Denton (FIG. 1) discloses, inter alia, a thin film transistor, comprising: a substrate; [and] a gate electrode (polysilicon bottom gate) disposed in the substrate..." Examiner further states that "Hiramatsu (FIG. 1) discloses a gate electrode 2, which is made of Ta or MoTa (column 3, lines 25-26) in order to increase conductivity of the semiconductor gate electrode." Examiner still further states that "Honda (FIG. 9) discloses a display device including a plurality of thin film transistors."

In response to the rejection, applicant has amended claim 11. Applicant asserts that the rejected claims are now patentable, as follows:

Amended claim 11 recites in pertinent part a display device including: a plurality of thin film transistors, each of the thin film transistors comprising a transparent substrate; and **a gate electrode made of metallic material, the gate electrode being disposed in the transparent substrate.**

Firstly, the thin film transistor disclosed by Denton comprises a bottom gate disposed in a substrate and made of polysilicon, whereas the thin film transistor of amended claim 11 comprises **a gate electrode being made of metallic material, with the gate electrode being disposed in the transparent substrate.** Secondly, the thin film transistor disclosed by Denton further comprises a top gate. That is, the thin film transistor disclosed by Denton is a dual-gated thin film transistor controlled by a top gate and a bottom gate, whereas the thin film transistor of amended claim 11 is a thin film transistor controlled by a single gate electrode. These differences indicate that Denton does not teach a thin film transistor comprising all the limitations recited in amended claim 11.

Further, Hiramatsu does not disclose a thin film transistor including **a gate electrode disposed in a transparent substrate**.

Therefore, there is no motivation or suggestion in either Denton or Hiramatsu that the reference be combined with the other in such a way as to provide each of the thin film transistors of amended claim 11.

Even though Honda discloses a display device including a plurality of thin film transistors, Honda does not provide any additional teaching to the teachings of Denton or Hiramatsu which might lead one of ordinary skill in the art to provide each of the thin film transistors of amended claim 11.

Therefore, there is no motivation or suggestion in any of Denton, Hiramatsu or Honda that the reference be combined with the other in such a way as to provide a display device comprising all the limitations recited

in amended claim 11.

Moreover, the display device of amended claim 11 produces new and unexpected results. That is, in each of the thin film transistors, **the gate electrode made of metallic material is deposited in the transparent substrate**, and thus the thickness of the gate electrode can be changed by changing the depth of the transparent substrate etched. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that each of the thin film transistors of amended claim 11 can efficiently reduce an RC delay of a scanning signal. Compare this with Denton, wherein the polysilicon backgate has applications as a bias to dynamically shift topgate threshold voltage for low power circuits.

Further, because the thickness of the gate electrode can be increased to reduce its impedance, an area of the gate electrode can be reduced without affecting the impedance of the gate electrode. Accordingly, an area of the pixel electrode may be increased, and thus the display device of amended claim 11 can obtain a higher aperture ratio.

Accordingly, amended claim 11 is submitted to be unobvious and patentable over Denton in view of Hiramatsu and further in view of Honda. Reconsideration and withdrawal of the rejection and allowance of amended claim 11 are respectfully requested.

Claim 12 depends from independent amended claim 11, and therefore should also be allowable.

Newly added claims 22 and 23 depend from amended independent claim 1. Accordingly, new claims 22 and 23 are submitted to be

patentable, and allowance thereof is respectfully requested.

Newly added claims 24 and 25 depend from amended independent claim 11. Accordingly, new claims 24 and 25 are submitted to be patentable, and allowance thereof is respectfully requested.

Newly added claims 26 and 27 depend from amended independent claim 21. Accordingly, new claims 26 and 27 are submitted to be patentable, and allowance thereof is respectfully requested.

In view of the foregoing, the present application as claimed in the pending claims is considered to be in a condition for allowance, and an action to such effect is earnestly solicited.

Respectfully submitted,
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